IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-PM00005

Inventor(s): Krishnaswamy Ramkumar, Kaichiu Wong and Venuka Jayatilaka

Serial No.:

Group Art Unit:

Filed: 08/09/00

Examiner:

Title: PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,468,676	TRENCH ISOLATIONS STRUCTURE AND METHOD FOR FORMING	11/21/95
5,858,858	ANNEALING METHODS FOR FORMING ISOLATION TRENCHES	01/12/99
5,910,018	TRENCH EDGE ROUNDING METHOD AND STRUCTURE FOR TRENCH ISOLATION	06/08/99
5,950,096	PROCESS FOR IMPROVING DEVICE YIELD IN INTEGRATED CIRCUIT FABRICATION	09/08/99
5,960,299	METHOD OF FABRICATING A SHALLOW-TRENCH ISOLATION STRUCTURE IN INTEGRATED CIRCUIT	09/28/99
5,994,178	METHOD OF FABRICATING CMOS TRANSISTORS WITH A PLANAR SHALLOW TRENCH ISOLATION	11/30/99
6,001,706	METHOD FOR MAKING IMPROVED SHALLOW TRENCH ISOLATION FOR SEMICONDUCTOR INTEGRATED CIRCUITS	12/14/99
6,004,864	ION IMPLANT METHOD FOR INTEGRATED CIRCUIT DEVICES	12/21/99
6,005,279	TRENCH EDGE SPACER FORMATION	12/21/99
6,013,561	METHOD FOR FORMING FIELD OXIDE FILM OF SEMICONDUCTOR DEVICE	01/11/00
6,020,251	METHOD OF FORMING BURIED DIFFUSION JUNCTIONS IN CONJUNCTION WITH SHALLOW-TRENCH ISOLATION STRUCTURES IN A SEMICONDUCTOR DEVICE	02/01/00
6,033,968	METHOD FOR FORMING A SHALLOW TRENCH ISOLATION STRUCTURE	03/07/00
6,037,018	SHALLOW TRENCH ISOLATION FILLED BY HIGH DENSITY PLASMA CHEMICAL VAPOR DEPOSITION	03/14/00

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 8/9/2000

By: _____
Anthony C. Murabito
Reg. No. 35,295